

**REMARKS**

The finality of the election requirement is noted. It is respectfully requested that the non-elected claims 4 and 6 be retained in this Application, during the pendency thereof, for possible rejoinder and/or for filing a divisional application. A divisional application already has been filed for non-elected claims 7-15; claims 7-15 have been canceled in this Application.

Claim 1 has been amended to more closely conform with U.S. claiming practice and to clarify the invention over the art. Claim 5 also has been amended to clarify the invention. No new matter has been entered.

Turning to the rejection of claims 1-3 and 5 under 35 USC §102 as anticipated by Hino et al. (U.S. Patent No. 6,157,084), claim 1 has been amended to specify that the semiconductor chip is "mounted so as to contact said first dielectric film." Hino et al. does not teach this feature. As is shown in Hino et al., semiconductor chip 11 contacts electrodes 12 and insulating resin layer 4. Thus, Hino et al. cannot anticipate claim 1 nor claims 2, 3 and 5 which depend thereon.

New claims 16-19 have been added to further scope the elected invention. New claims 16-19 define that the second interconnect pattern 14 is disposed directly in contact with the encapsulating resin 18, which the cited reference does not teach.

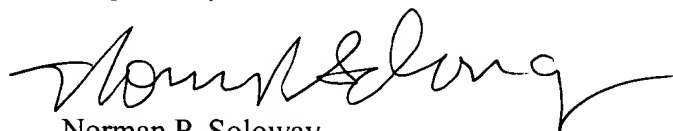
Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action are respectfully requested.

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Respectfully submitted,



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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP - NON-FEE AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 27, 2004, at Tucson, Arizona.

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